

AMENDMENTS TO CLAIMS:

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12. (Currently Amended) The method of signal processing according to claim ~~11~~ 22, wherein the value of the delayed second component during each of the series of time periods is based on (A) the value of the second component during the time period and the (B) value of the second component during at least one time period adjacent to the time period.

13. (Currently Amended) The method of signal processing according to claim ~~11~~ 22, wherein the series of time periods comprises a series of consecutive time periods of equal duration.

14. (Original) The method of signal processing according to claim 13, wherein the fractional delay is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and

wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period.

15. (Original) The method of signal processing according to claim 14, wherein the fractional portion is substantially equal to one-half of a time period.

16. (Currently Amended) The method of signal processing according to claim ~~14~~ 22, wherein a boundary between each of the series of time periods is defined by a transition of a clock signal.

17. (Original) The method of signal processing according to claim 16, wherein a duty cycle of the clock signal is substantially equal to fifty percent.

18. (Currently Amended) The method of signal processing according to claim ~~14~~ 22, wherein the values multiplexed onto the common signal path are n bits wide, and wherein the common signal path is less than $2n$ bits wide.

19. (Currently Amended) The method of signal processing according to claim ~~14~~ 22, wherein the values multiplexed onto the common signal path are n bits wide, and wherein the common signal path is n bits wide.

20. (Currently Amended) The method of signal processing according to claim ~~14~~ 22, further comprising producing a delayed first component based on the first component and having an integer delay with respect to the first component.

wherein multiplexing the values of the delayed second component and the values of a component based on the first component onto a common signal path includes multiplexing the values of the delayed second component and the values of the delayed first component onto a common signal path.

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22. (Currently Amended) A method of signal processing comprising:

receiving a composite signal having a first component and a second component, the first component including a series of values, each value of the first component being constant over substantially an entire corresponding one of a series of time periods, the second component including a series of values, each value of the second component being constant over substantially an entire corresponding one of the series of time periods;

producing a delayed second component based on the second component and having a fractional delay with respect to the second component, the delayed second component including a series of values, each value of the delayed second component being constant over substantially an entire corresponding one of the series of time periods;

multiplexing the delayed second component and the values of a component based on the first component onto a common signal path;

[The method of signal processing according to claim 11, further comprising:]

demultiplexing the values of the delayed second component and the values of the component based on the first component from the common signal path to produce a transferred first component based on the first component and a transferred second component based on the second component; and

producing a first analog component based on the transferred first component and a second analog component based on the transferred second component.

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31. (Currently Amended) The device according to claim 30 35, wherein the common signal path includes a plurality of terminals of a chip package that includes the device.

32. (Currently Amended) The device according to claim 30 35, further comprising a delay configured and arranged to receive the first component and to output a delayed first component based on the first component,

wherein the multiplexer is configured and arranged to receive the delayed first component.

33. (Currently Amended) The device according to claim 30 35, wherein the first component and the second component are synchronous to a clock signal, and wherein a length of a delay of the delayed second component with respect

to the second component is measured in durations of a period of the clock signal and includes an integer portion and a nonzero fractional portion, and

wherein the fractional portion is at least one-quarter of a period of the clock signal and no greater than three-quarters of a period of the clock signal.

34. (Currently Amended) The device according to claim 30 35, wherein the fractional portion is substantially equal to one-half of a period of the clock signal.

35. (Currently Amended) A device configured and arranged to output a multiplexed signal based on an original composite signal having a first component and a second component, comprising:

a common signal path configured and arranged to carry the multiplexed signal;

a multiplexer configured and arranged to receive (A) a component based on the first component and (B) a delayed second component based on the second component and to produce the multiplexed signal; and

a filter configured and arranged to receive the second component and to produce the delayed second component.

[The device according to claim 30, wherein]

the filter [includes] including a shifter configured and arranged to receive an input value and to output a shifted value, wherein the shifted value is equal to 2^i times the input value, where i is an integer, and wherein a value of the delayed second component is based on the shifted value.

36. (Currently Amended) A device configured and arranged to output a multiplexed signal based on an original composite signal having a first component and a second component, comprising:

a common signal path configured and arranged to carry the multiplexed signal;

a multiplexer configured and arranged to receive (A) a component based on the first component and (B) a delayed second component based on the second component and to produce the multiplexed signal; and

a filter configured and arranged to receive the second component and to produce the delayed second component.

[The device according to claim 30, wherein]

wherein a transfer function of the filter is expressible as

$$(-1/16)z + (9/16)z^{-1} + (9/16)z^{-2} + (-1/16)z^{-3}.$$

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38. (Currently Amended) The system according to claim 37 39, further comprising a modulator configured and arranged to modulate an in-phase component of a carrier with a component based on the transferred first component and a quadrature component of the carrier with a component based on the transferred second component.

39. (Currently Amended) A system comprising:

a device configured and arranged to output a multiplexed signal based on an original composite signal having a first component and a second component, the device including:

a common signal path configured and arranged to carry the multiplexed signal,

a multiplexer configured and arranged to receive (A) a component based on the first component and (B) a delayed second component based on the second component and to produce the multiplexed signal, and

a filter configured and arranged to receive the second component and to produce the delayed second component;

a demultiplexer configured and arranged to receive the multiplexed signal and to produce a transferred first component based on the first component and a transferred second component based on the delayed second component, the delayed second component being synchronous to the first component and having a fractional delay with respect to the second component; and

[The system according to claim 37, further comprising]

a first digital-to-analog converter configured and arranged to produce a first analog component based on the transferred first component and a second digital-to-analog converter configured and arranged to produce a second analog component based on the transferred second component.